



THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

**DeWitt, Jr. et al.**

Serial No: **10/675,751**

Filed: **September 30, 2003**

Title: **Method and Apparatus for  
Monitoring Processing of Instructions and  
Memory Locations in a Data Processing  
System**

Group Art Unit: **2183**

Intellectual Property  
Law Department  
International Business  
Machines Corporation  
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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
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Sir:

Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. 1.56.

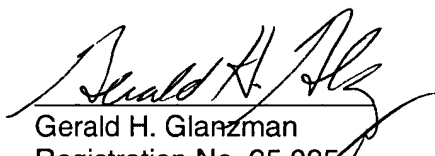
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No item of information cited in this Supplemental Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in this Supplemental Information Disclosure Statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of this Supplemental Information Disclosure Statement.

In the event a fee is required in connection with the enclosed Supplemental Information Disclosure Statement, the Commissioner of Patents and Trademarks is authorized to charge Deposit Account No. 09-0447 for the necessary amount.

Respectfully submitted,



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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT****Complete if Known**

Application Number	10/675,751
Filing Date	09/30/2003
First Named Inventor	DeWitt, Jr. et al.
Examiner Name	Cody, Dillon J.
Art Unit	2183
Attorney Docket No.	AUS920030482US1

Examiner Initials	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
AA	5,710,881	01-20-1998	Gupta et al.	
AB	5,822,763	10-13-1998	Baylor et al.	
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**FOREIGN PATENT DOCUMENTS**

Examiner Initial	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

**NON PATENT LITERATURE**

Examiner Initial	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
AN	TANENBAUM, "Structured Computer Organization", 1984, Prentice-Hall, Inc., 2 <sup>nd</sup> Edition, pp. 10-12.
AO	TORRELLAS et al., "False Sharing and Spatial Locality in Multiprocessor Caches", June 1994, IEEE Transactions on Computers, Vol. 43, No. 6, pp. 651-663.
AP	ROTHMAN et al., "Analysis of Shared Memory Misses and Reference Patterns", 2000, IEEE, pp. 187-198.
AQ	Wikipedia "JavaServer Pages" downloaded 1/24/06 <a href="http://en.wikipedia.org/wiki/JavaServer_Pages">http://en.wikipedia.org/wiki/JavaServer_Pages</a>
AR	"Hardware Cycle Based memory Residency", IBM, May 22, 2003, ip.com, IPCOM000012728D, pp. 1-2
AS	HYDE, "The Art of Assembly Language", 2001, Linux Edition, pp. 247-248, retrieved Mar. 1, 2005 from <a href="http://webster.cs.ucr.edu/AoA/Linux/PDFs/0_PDFIndexLinux.html">http://webster.cs.ucr.edu/AoA/Linux/PDFs/0_PDFIndexLinux.html</a>

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